

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : David Lewis

Application No. : 10/723,530 Confirmation No.: Not yet

assigned

Filed : November 24, 2003

For : LOGIC DEVICE LOGIC MODULES HAVING

IMPROVED ARITHMETIC CIRCUITRY

Group Art Unit : Not yet assigned

New York, New York 10020

 $\{ (x_i, x_i) \in \mathcal{X}_{i+1} = \emptyset \}$

February 17, 2004

Hon. Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicant hereby makes the following references of record in the above-identified patent application:

U.S. Patents

5,258,668	Cliff et al.	11/02/93
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5,274,581	Cliff et al.	12/28/93
5,295,090	Hsieh et al.	03/15/94
5,349,250	New	09/20/94
5,359,242	Veenstra	10/25/94
5,365,125	Goetting et al.	11/15/94
5,481,206	New et al.	01/02/96
5,481,486	Cliff et al.	01/02/96
5,483,478	Chiang	01/09/96
5,500,608	Goetting et al.	03/19/96
5,523,963	Hsieh et al.	06/04/96
5,546,018	New et al.	08/13/96
5,629,886	New	05/13/97
5,631,576	Lee et al.	05/20/97
5,672,985	Lee	09/30/97
5,675,262	Duong et al.	10/07/97
5,724,276	Rose et al.	03/03/98
5,761,099	Pederson	06/02/98

5,818,255	New et al.	10/06/98
5,889,411	Chaudhary	03/30/99
5,898,318	Pederson	04/27/99
5,898,319	New	04/27/99
5,898,602	Rothman et al.	04/27/99
6,107,827	Young et al.	08/22/00
6,154,052	New	11/28/00
6,154,053	New	11/28/00
6,157,209	McGettigan	12/05/00
6,288,570	New	09/11/01
6,359,468	Park et al.	03/19/02
6,427,156	Chapman et al.	07/30/02
6,480,023	Kaviani	11/12/02
6,529,040	Carberry et al.	03/04/03

U.S. Patent Applications

10/195,209	Kaptanoglu et al.	filed	07/12/02
10/280,723	Lewis et al.	filed	10/24/02

Other Documents

Altera Corporation, "Stratix Device Handbook, Volume 1," July 2003, pp. 1-1 - 1-2, 2-3 - 2-14.

Xilinx, Inc., "Virtex-II Platform FPGAs: Introduction and Overview," Product Specification, Version 2.0, August 1, 2003, p. 1.

Xilinx, Inc., "Virtex-II Platform FPGAs: Detailed Description," Product Specification, Version 3.0, August 1, 2003, pp. 12-18.

Copies of all of the aforementioned references, which are also listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

It is respectfully requested that these references be (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form

PTO-1449, as considered and initialed by the Examiner, be returned with the next communication.

An early and favorable action is respectfully requested.

Respectfully submitted,

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Claire J Samue an Goodman

Alexandria, VA 22313-1450 on

Signature of Person Signing

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

ATTY. DOCKET NO. 174/304	APPLN. NO. 10/723,530
APPLICANT David Lewis	CONF. NO. Not yet assigned
FILING DATE November 24, 2003	GROUP ART UNIT Not yet assigned

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING I IF APPROP	
	5,258,668	11/02/93	Cliff et al.	307	465		
	5,274,581	12/28/93	Cliff et al.	364	784		
	5,295,090	03/15/94	Hsieh et al.	364	784		
	5,349,250	09/20/94	New	307	465		
	5,359,242	10/25/94	Veenstra	307	465		
	5,365,125	11/15/94	Goetting et al.	326	39		
	5,481,206	01/02/96	New et al.	326	38		
	5,481,486	01/02/96	Cliff et al.	364	716		
	5,483,478	01/09/96	Chiang	364	787		
	5,500,608	03/19/96	Goetting et al.	326	39		
	5,523,963	06/04/96	Hsieh et al.	364	786		
	5,546,018	08/13/96	New et al.	326	38		
	5,629,886	05/13/97	New	364	787		
	5,631,576	05/20/97	Lee et al.	326	39		
	5,672,985	09/30/97	Lee	326	41		
	5,675,262	10/07/97	Duong et al.	326	41		
	5,724,276	03/03/98	Rose et al.	364	716.06		
		FOREIGN	PATENT DOCUM	MENTS			
EXAMINER	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSL YES	ATION NO
INITIAL				·····	-	123	110
							
	OTHER DOCUMEN	I———— ITS (Includii	ng Author, Title, I	Date, Pertine	nt Pages, Etc.)	
EXAMINER INITIAL							
	Altera Corporation, "Stra						
	Xilinx, Inc., "Virtex-II Plat 2.0, August 1, 2003, p. 1		s: Introduction an	d Overview,	' Product Spec	ification, Ver	sion
	Xilinx, Inc., "Virtex-II Plat August 1, 2003, pp. 12-1	form FPGA	s: Detailed Descr	ipton," Produ	uct Specificatio	n, Version 3.	0,

EXAMINER

DATE CONSIDERED

INFORMATION DISCLOSURE STATEMENT BY APPLICANT			David Lewis FILING DATE November 24, 2003		Not yet assigned GROUP ART UNIT Not yet assigned		
BADEMARK		U.S.	PATENT DOCUME	NTS			
EXAMINER NITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING IF APPROF	
	5,761,099	06/02/98	Pederson	364	716.01		<u>-</u>
	5,818,255	10/06/98	New et al.	326	39		
	5,889,411	03/30/99	Chaudhary	326	39		
	5,898,318	04/27/99	Pederson	326	39		
	5,898,319	04/27/99	New	326	41		
	5,898,602	04/27/99	Rothman et al.	364	716.01		
	6,107,827	08/22/00	Young et al.	326	41		
	6,154,052	11/28/00	New	326	41		
	6,154,053	11/28/00	New	326	41		
	6,157,209	12/05/00	McGettigan	326	39		
	6,288,570	09/11/01	New	326	41	<u> </u>	
-	6,359,468	03/19/02	Park et al.	326	39		
	6,427,156	07/30/02	Chapman et al.	708	235		
	6,480,023	11/12/02	Kaviani	326	38		
	6,529,040	03/04/03	Carberry et al.	326	40		
		U.S.	PATENT APPLICAT	IONS			
EXAMINER NITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	Appln. 10/195,209		Kaptanoglu et al.			07/12/02	
	Appln. 10/280,723		Lewis et al.			10/24/02	
		FOREI	GN PATENT DOCU	MENTS			
EXAMINER NITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSL YES	ATION NO
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